Massachusetts Institute of Technology

Negative-Bias Temperature Instability (NBTI) of GaN MOSFETs

Alex Guo and Jesús A. del Alamo

Microsystems Technology Laboratories (MTL)

Massachusetts Institute of Technology (MIT)

Cambridge, MA, USA

Sponsor: MIT/MTL Gallium Nitride (GaN) Energy Initiative

United States National Defense Science & Engineering Graduate Fellowship (NDSEG)

Purpose

To understand the physics of and to mitigate NBTI in GaN n-MOSFETs.

Outline

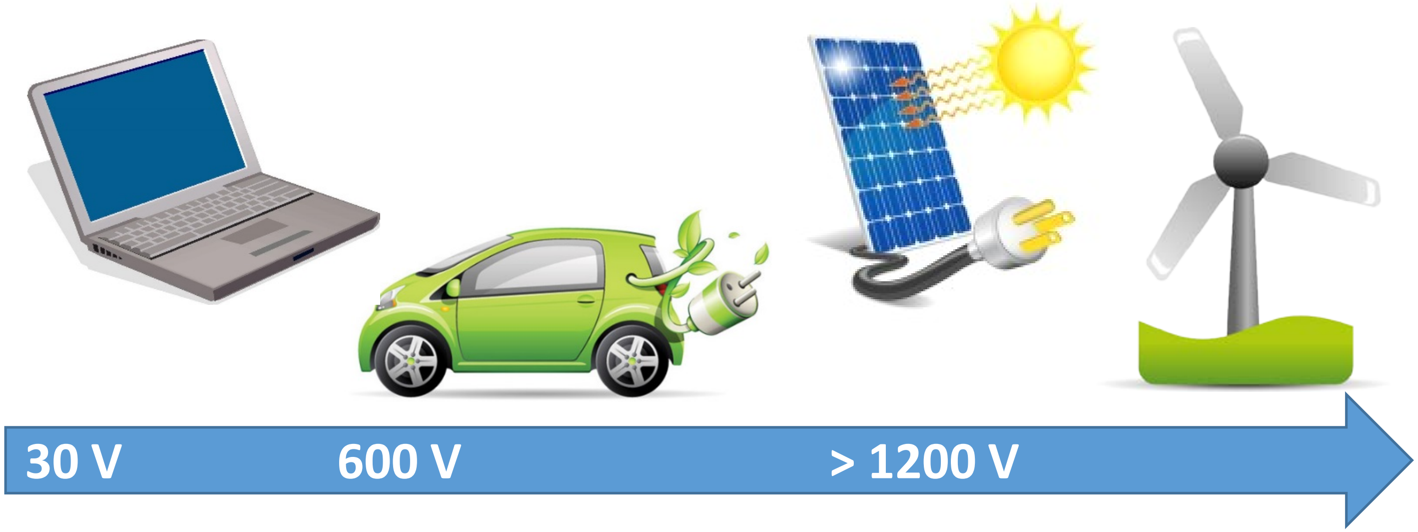
1. Motivation
2. Experimental setup
3. Three regimes of NBTI
4. Summary of contributions

Outline

1. **Motivation**
2. Experimental setup
3. Three regimes of NBTI
4. Summary of contributions

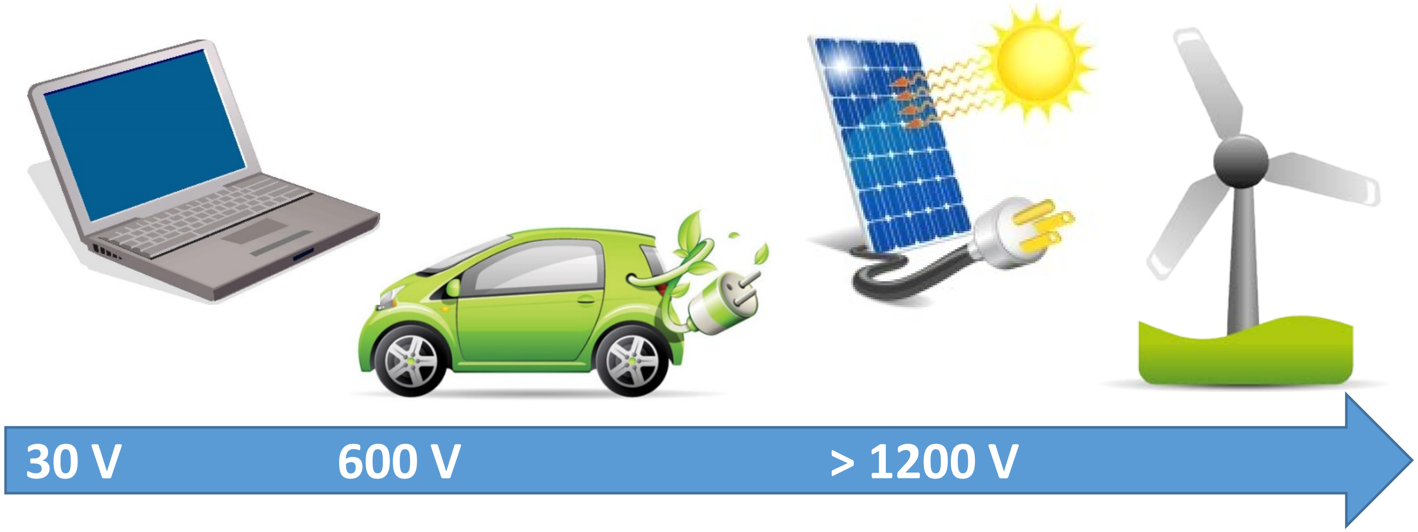
GaN for power electronics

- **Promising for a wide range of applications**



GaN for power electronics

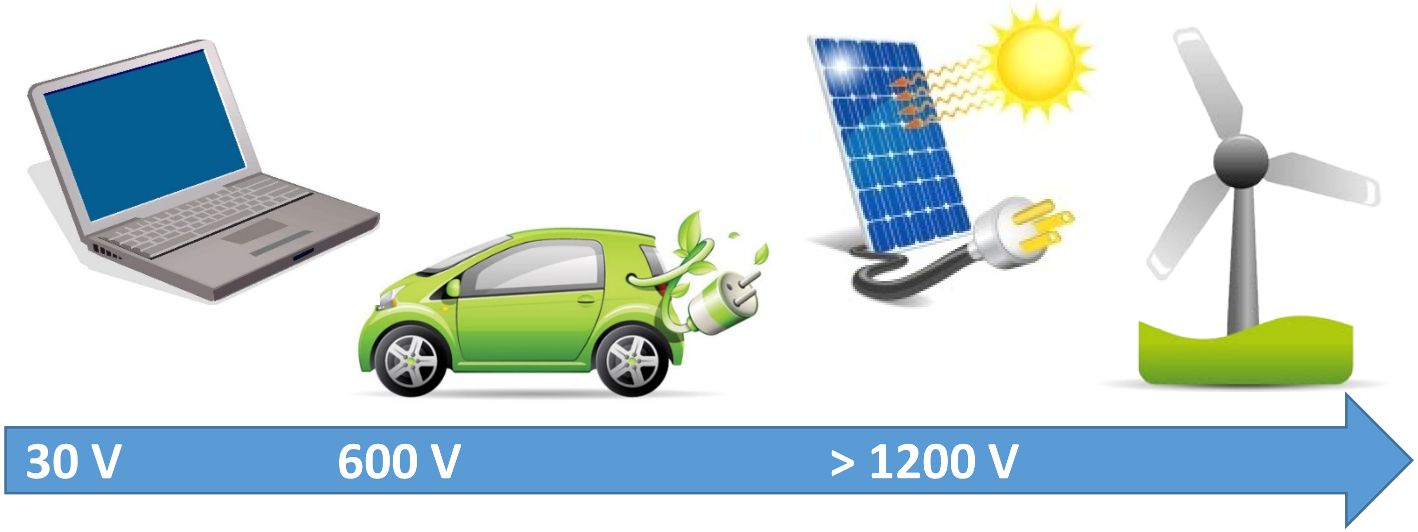
- **Promising for a wide range of applications**



- **Negative-Bias Temperature Instability (NBTI) is a major concern:**
  - **Operational instability**
  - **Long-term reliability**

GaN for power electronics

- **Promising for a wide range of applications**

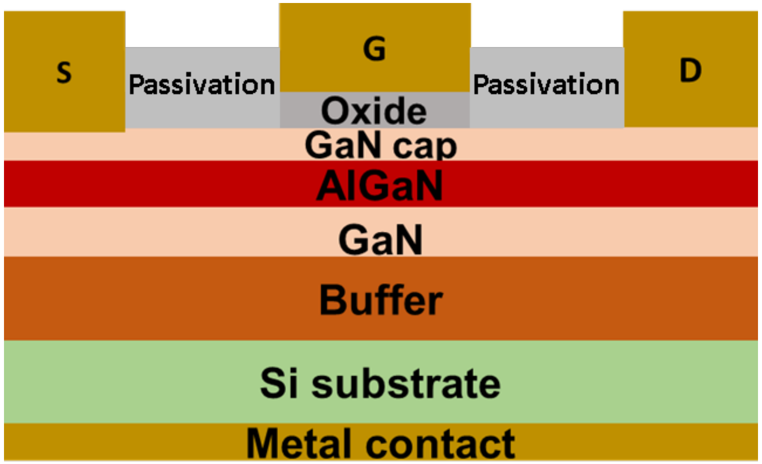


- **Negative-Bias Temperature Instability (NBTI) is a major concern:**
  - **Operational instability**
  - **Long-term reliability**

Challenge: mechanisms responsible for NBTI?

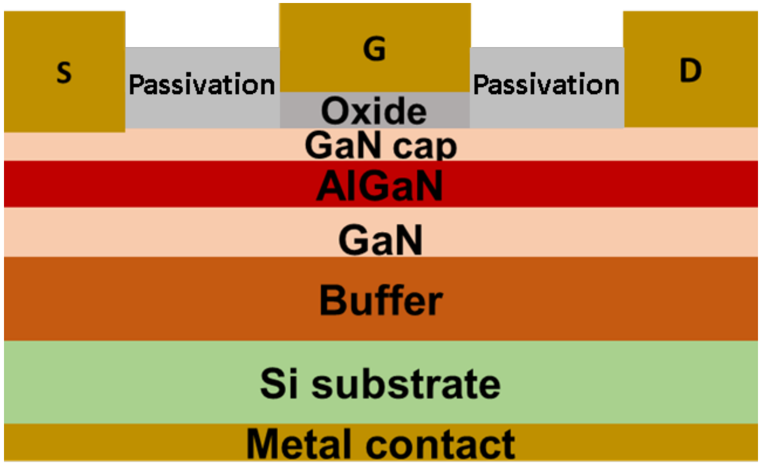
GaN MIS-HEMT for high voltage applications

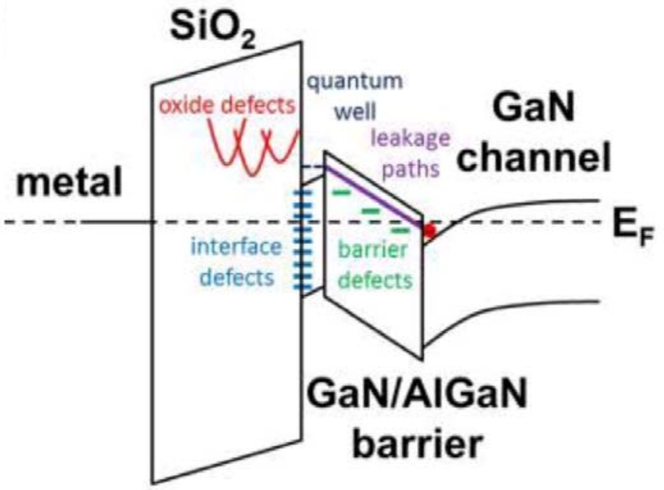
- **MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor**
- **Large gate swing, low gate leakage**



GaN MIS-HEMT for high voltage applications

- MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor
- Large gate swing, low gate leakage

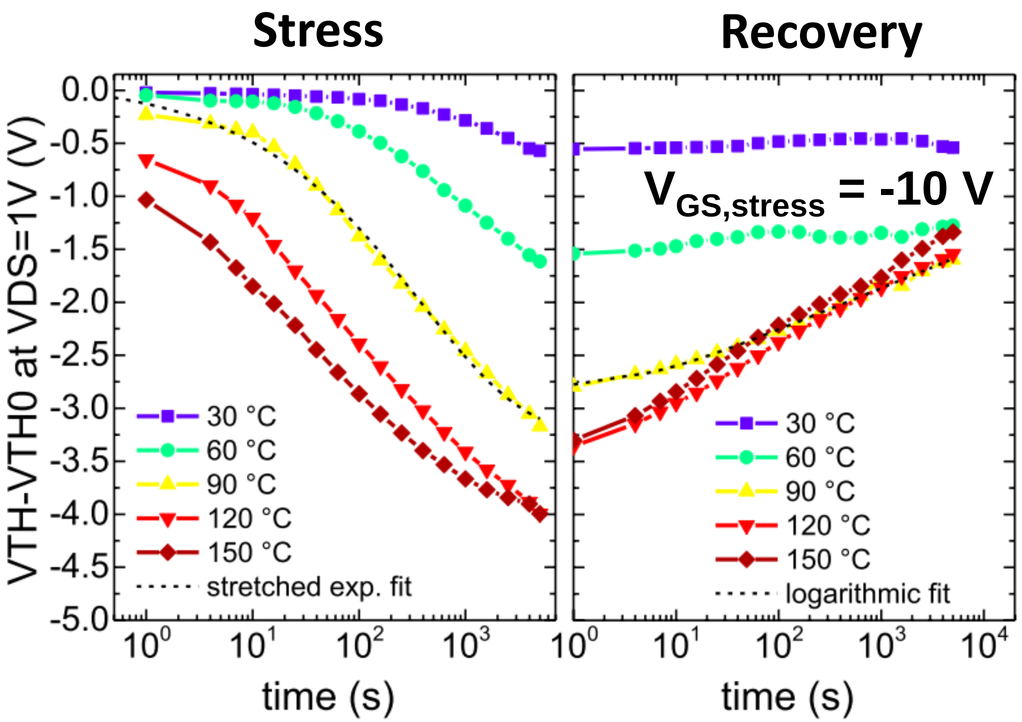




[Lagger, TED 2014]

- Presence of gate oxide brings new stability and reliability concerns not present in HEMTs

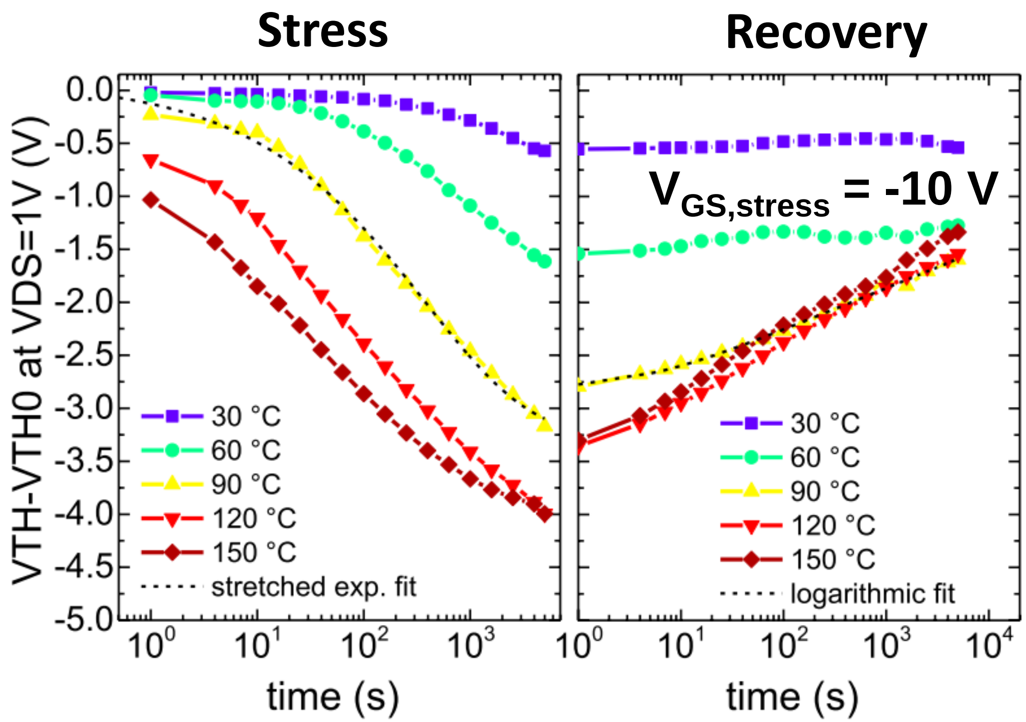
NBTI of GaN MIS-HEMT



[Meneghini, EDL 2016]

- Large $\Delta V_T < 0$ at moderate $V_{GS,stress}$, slow partial recovery
- Possible mechanism: trapping in multiple layers and interfaces

NBTI of GaN MIS-HEMT



[Meneghini, EDL 2016]

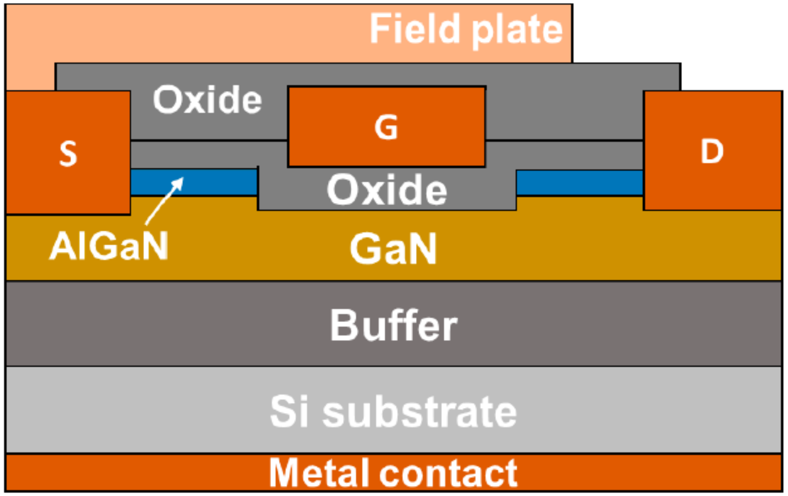
- **Large $\Delta V_T < 0$ at moderate $V_{GS,stress}$, slow partial recovery**
- **Possible mechanism: trapping in multiple layers and interfaces**

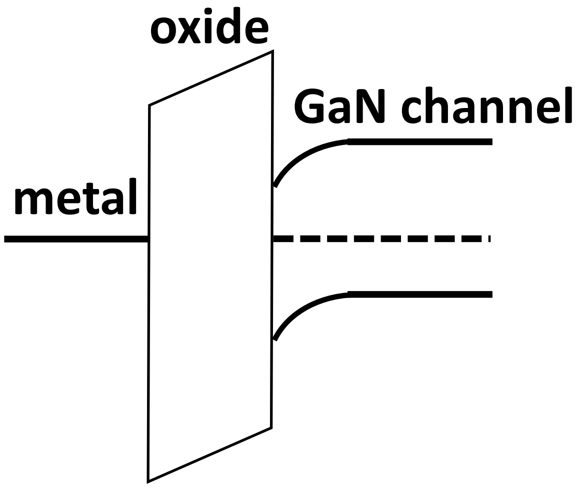
To better understand NBTI:

Stress voltage dependence ; dynamics of S and $g_{m,max}$; simpler structure

Simpler GaN MOSFET structure

- Industrial prototype devices
- SiO_2/Al_2O_3 composite gate dielectric, EOT = 40 nm





- Isolate oxide and oxide/GaN interface

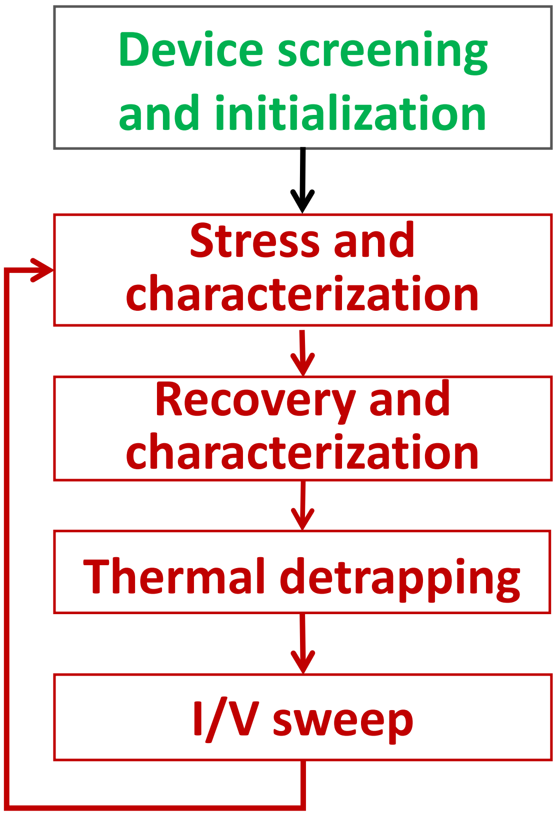
  IRPS 2015: PBTI

  This work: physical mechanisms behind NBTI of GaN MOSFET

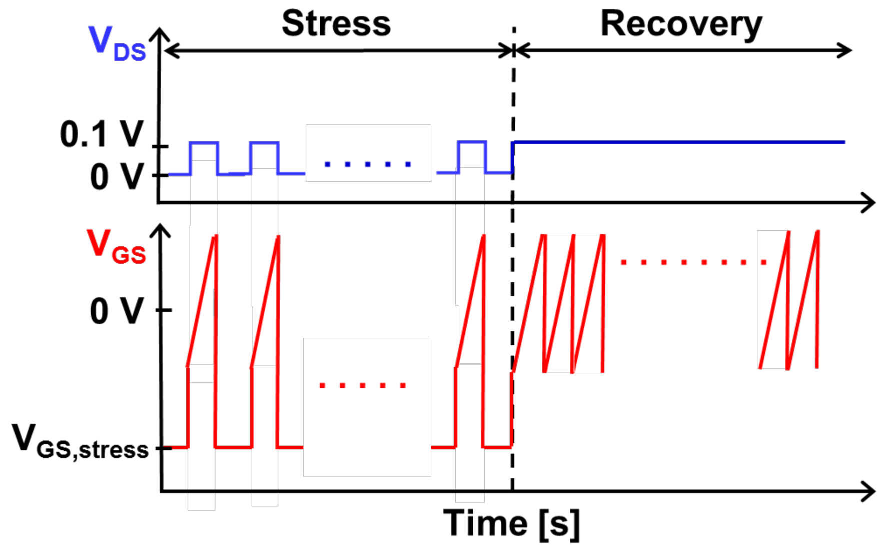
Outline

1. Motivation
2. **Experimental setup**
3. Three regimes of NBTI
4. Summary of contributions

Experiment flow and FOM definition



Increase stress voltage or temperature



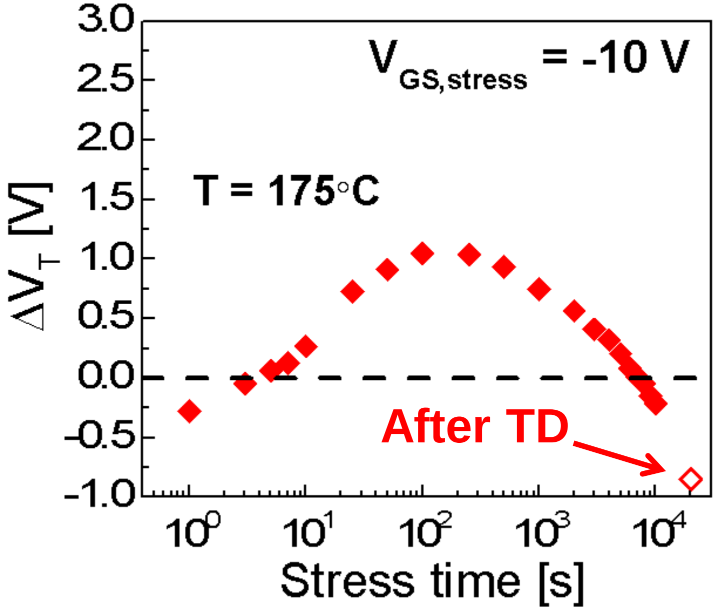
- V_T : V_{GS} value when I_D = 1 μA/mm
- S : Extracted at I_D = 0.1 μA/mm
- $g_{m,max}$: Extracted from I_{DS}-V_{GS} ramp
- All at V_{DS} = 0.1 V
- First sample: ~ 1- 2 s after removal of stress

Outline

1. Motivation
2. Experimental setup
3. **Three regimes of NBTI**
4. Summary of contributions

V_T shift overview

This work: GaN MOSFET



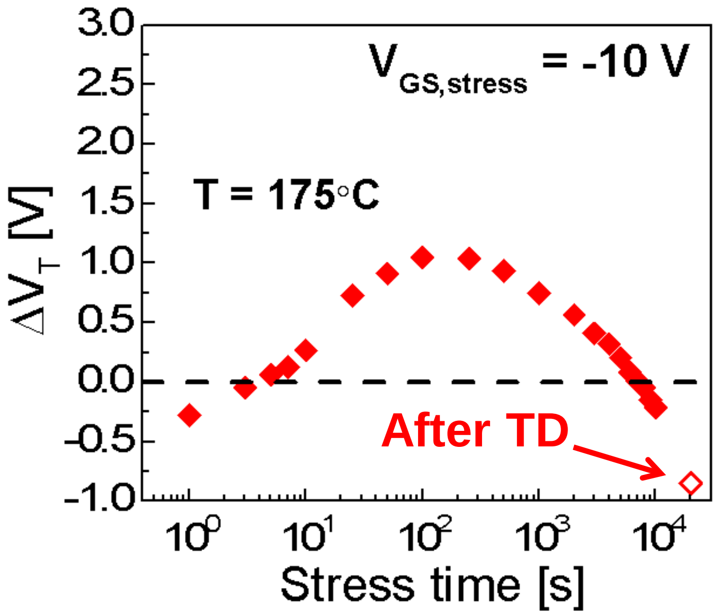
**TD: Thermal Detrapping*

<u>Three regimes:</u>

- **Small negative ΔV_T → positive ΔV_T → negative ΔV_T**
- **Permanent negative ΔV_T after TD**

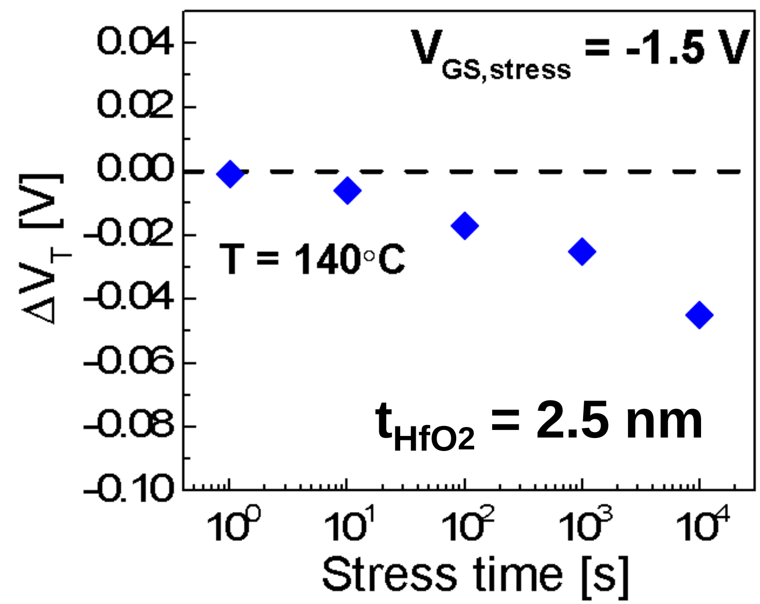
V_T shift overview

This work: GaN MOSFET



***TD: Thermal Detrapping**

Si HKMG p-MOSFET



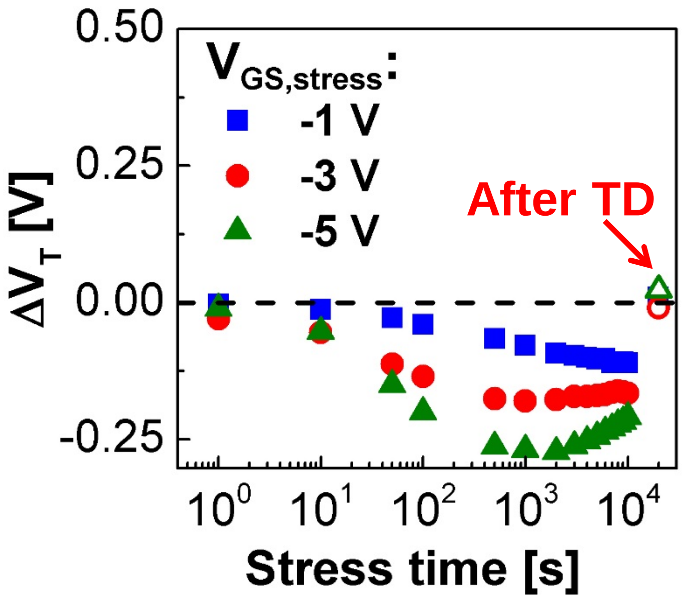
[Zafar, TDMR 2005]

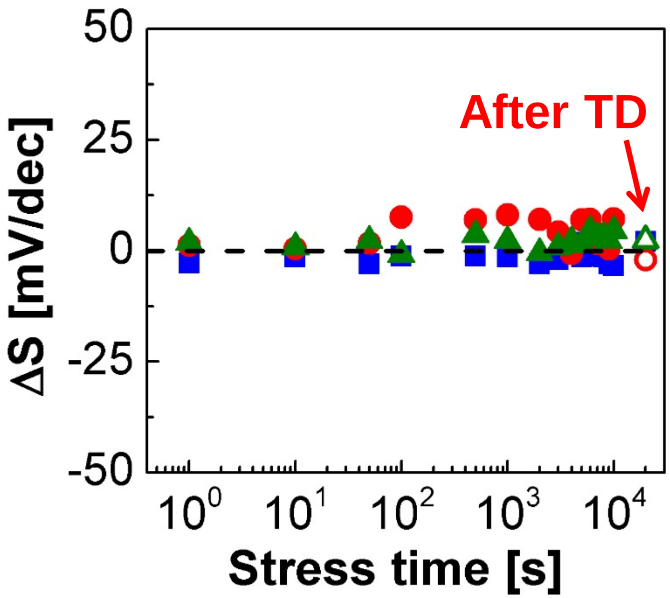
Three regimes:

- **Small negative ΔV_T → positive ΔV_T → negative ΔV_T**
- **Permanent negative ΔV_T after TD**

Regime 1 (low-stress)

Time evolution of ΔV_T and ΔS at RT



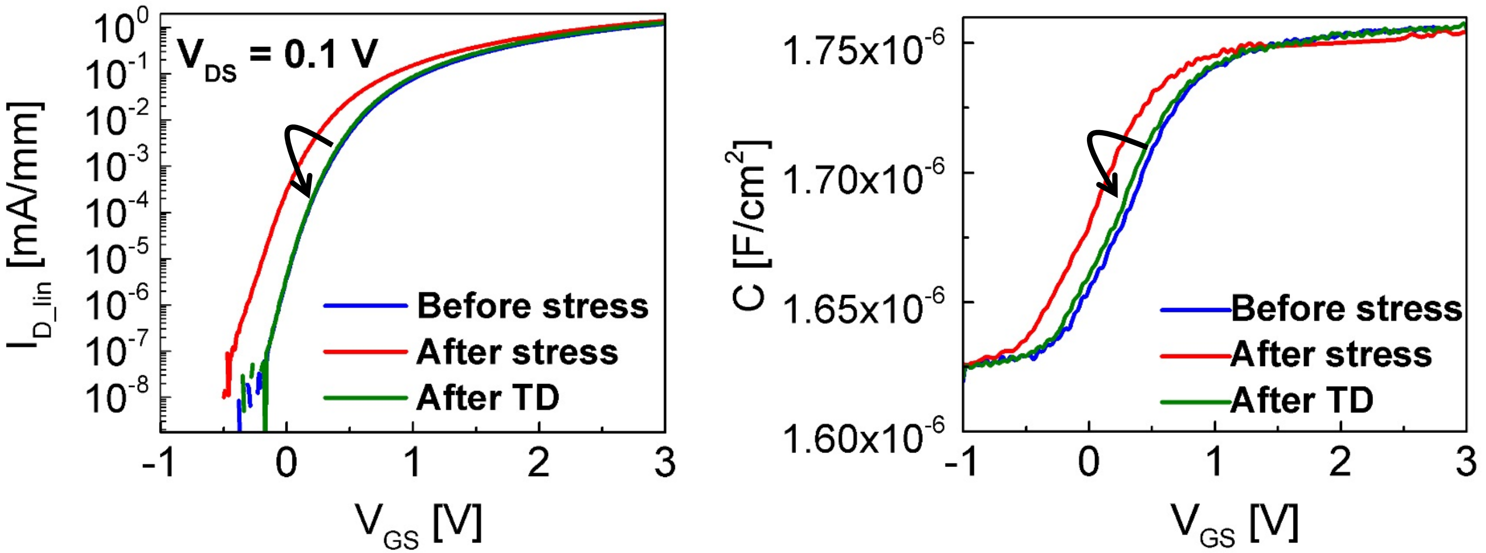


- **Negative ΔV_T, $|\Delta V_T|$ increases with t_{stress} and $|V_{GS,stress}|$**
- **Minimal ΔS**
- **Complete recovery**

Regime 1 (low-stress)

I_D-V_{GS} and C_G-V_G characteristics

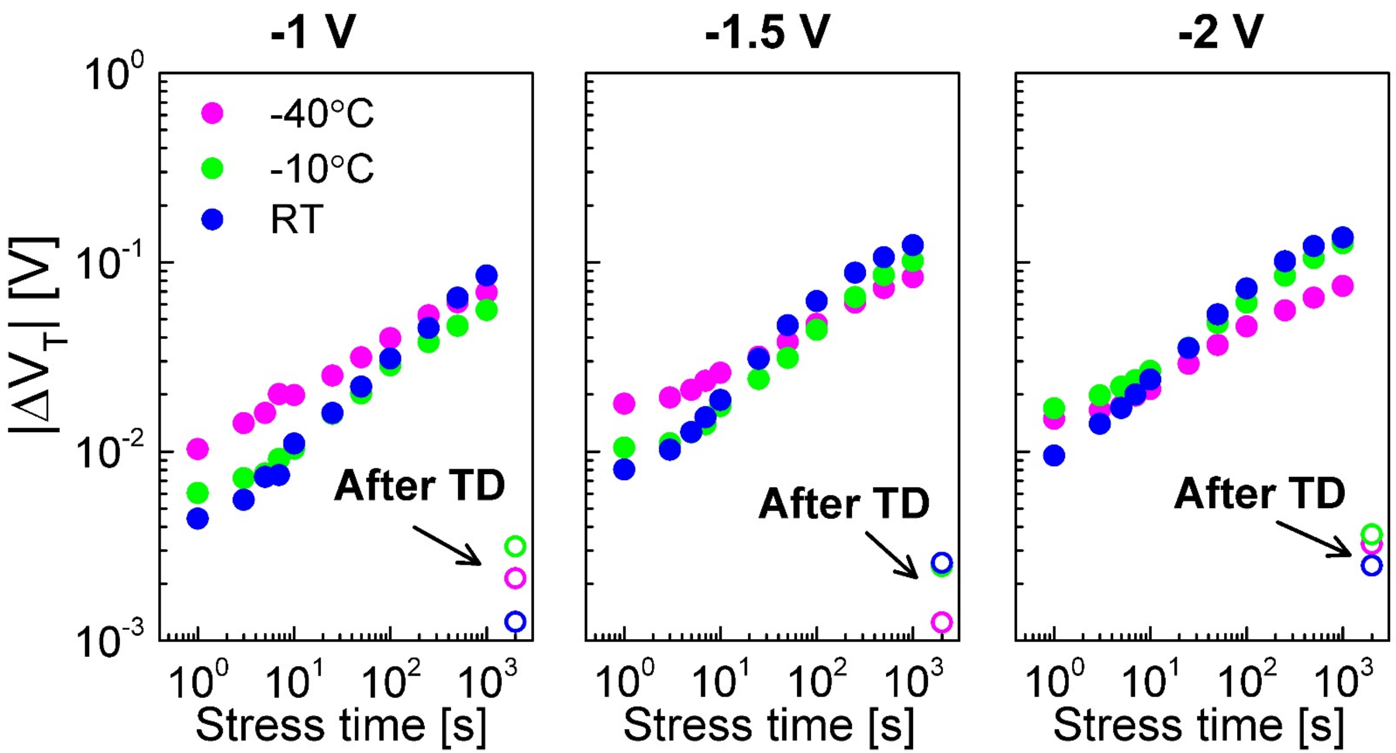
$V_{GS,stress}$ = -1 V, t_{stress} = 10,000, RT



- **Simple parallel V_T shift that completely recovers**

Regime 1 (low-stress)

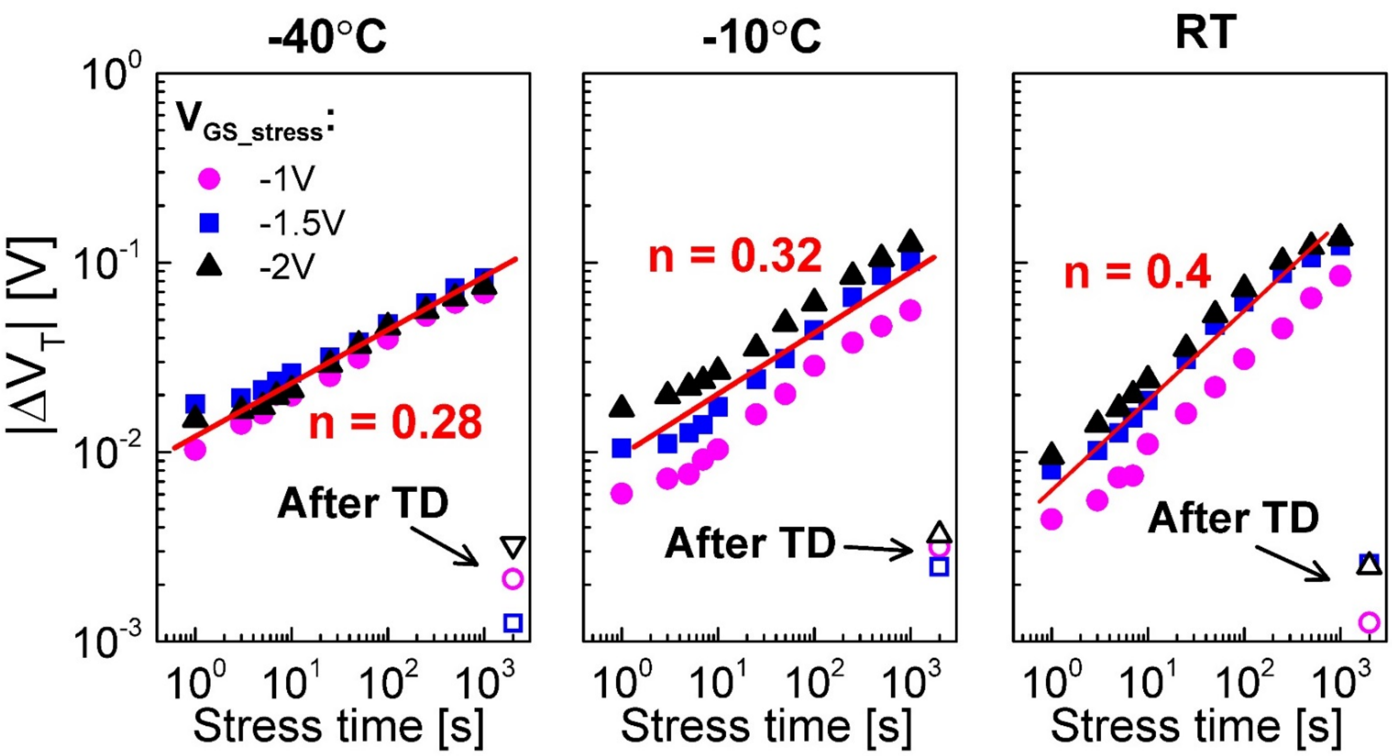
Temperature dependence



- **Rate of V_T shift shows slight positive T dependence**

Regime 1 (low-stress)

Modeling

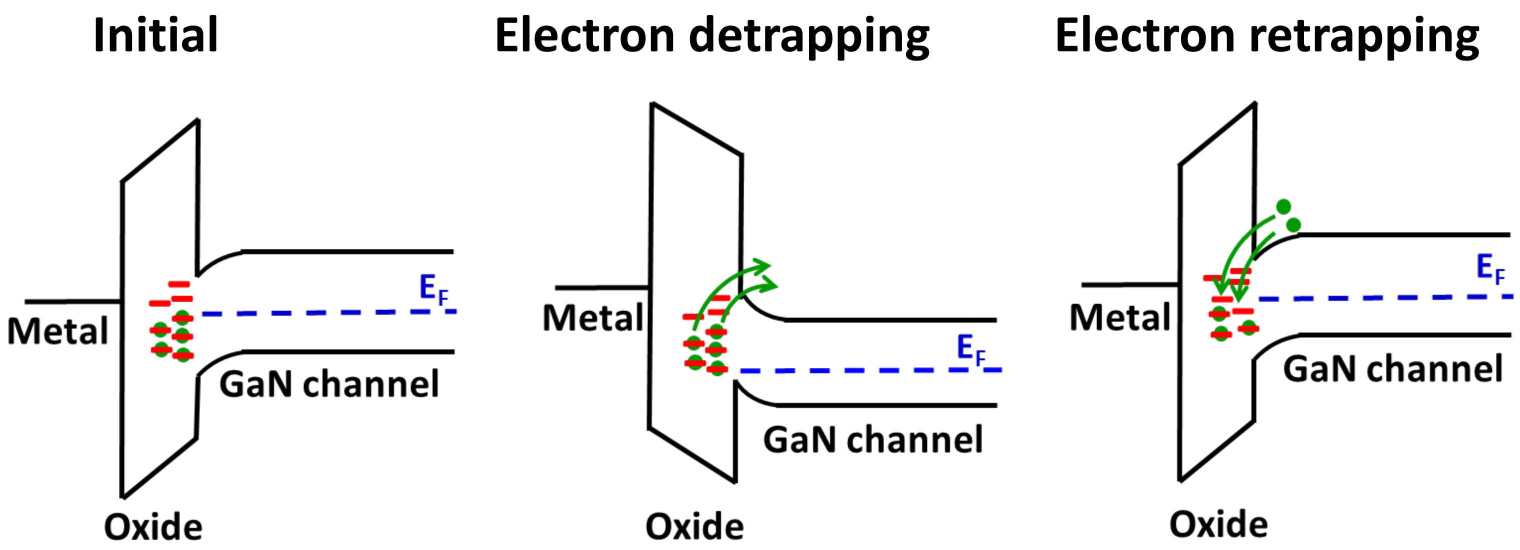


- **Power law with n = 0.28 to 0.4**
- **Similar to PBTI observation [Guo, IRPS 2015]**

Regime 1 (low-stress)

ΔV_T mechanism

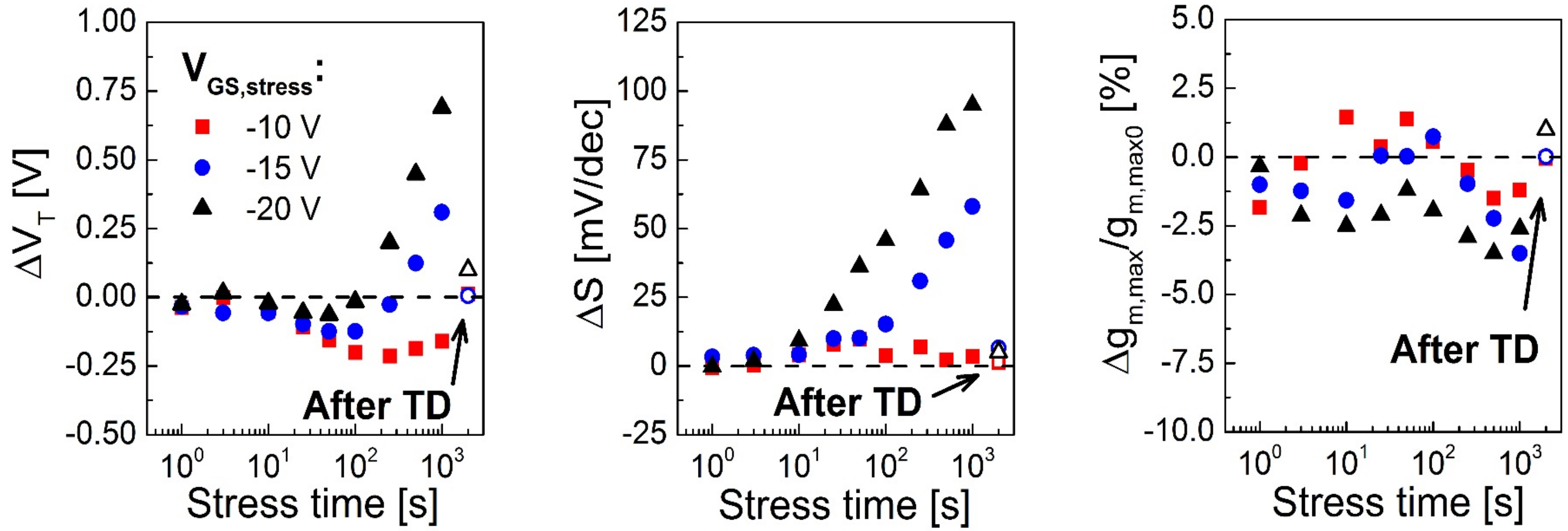
- Consistent with electron detrapping and retrapping from/to pre-existing oxide traps



- Also seen in Si HKMG MOSFETs [Young, IRWS 2003] and Al_2O_3/InGaAs MOSFETs [Wrachien, EDL 2011]

Regime 2 (mid-stress)

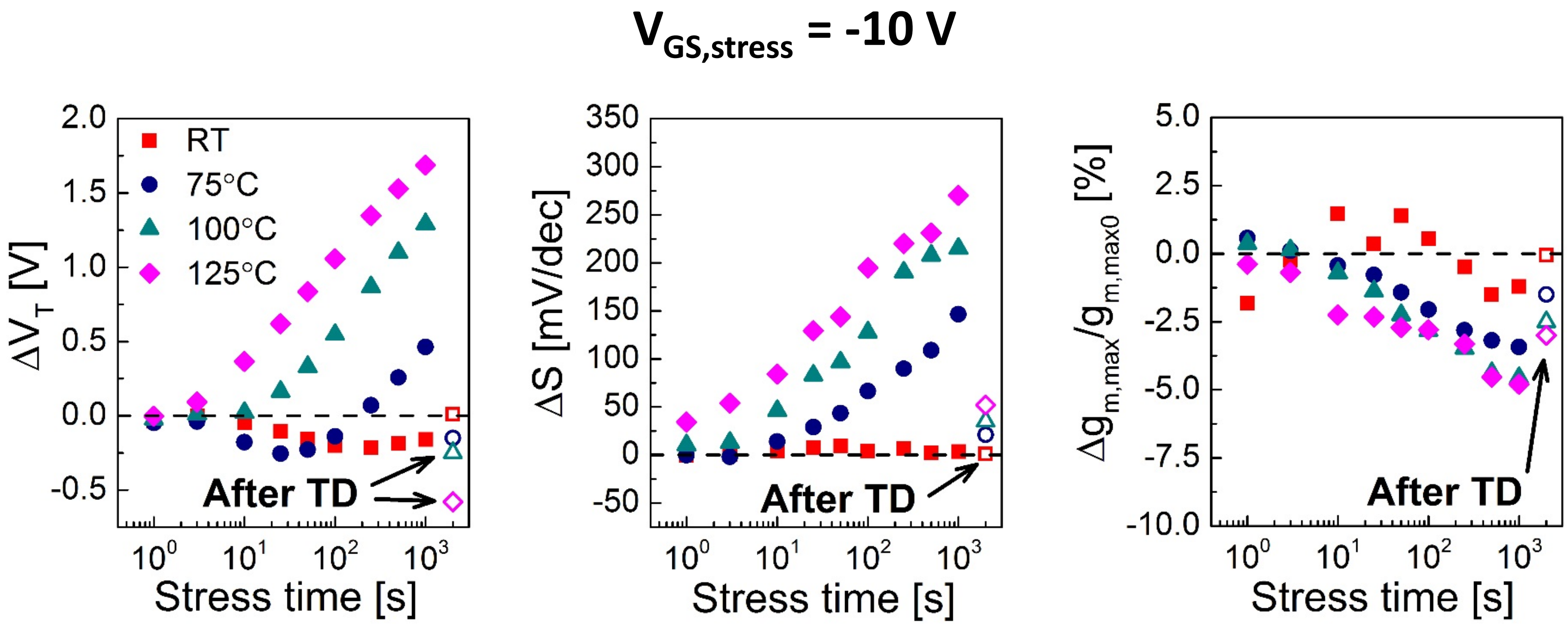
t_{stress} evolution of ΔV_T , ΔS and $\Delta g_{m,max}$ at RT



- $\Delta V_T > 0$
- $|V_{GS,stress}|\uparrow$, $t_{stress}\uparrow \rightarrow \Delta V_T \uparrow$, $\Delta S \uparrow$, $|\Delta g_{m,max}| \uparrow$
- ΔV_T , ΔS and $|\Delta g_{m,max}|$ mostly recoverable

Regime 2 (mid-stress)

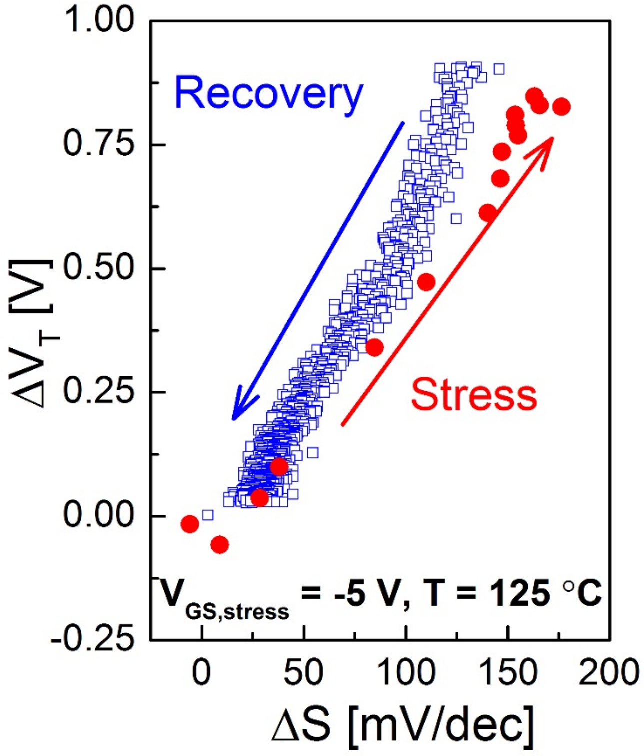
Temperature dependence



- **All parameter shifts enhanced by T**
- **At high T, recovery incomplete → transition to regime 3**

Regime 2 (mid-stress)

ΔV_T and ΔS correlation

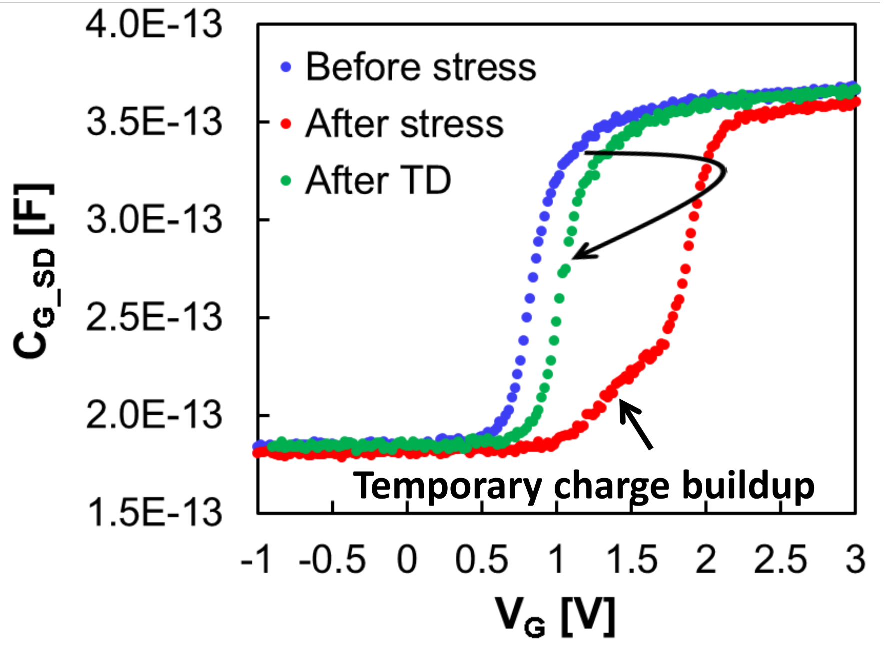


- ΔV_T and ΔS are linearly correlated throughout the entire experiment, and completely recover

Regime 2 (mid-stress)

C-V characteristics

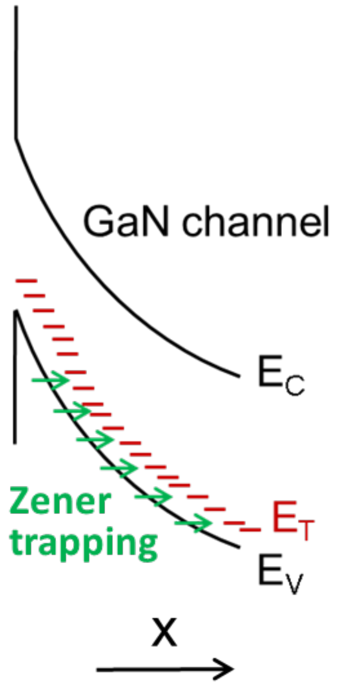
$V_{GS,stress}$ = -20 V, t_{stress} = 1,000 s, RT



- **Temporary charge buildup around threshold after stress**

Regime 2 (mid-stress)

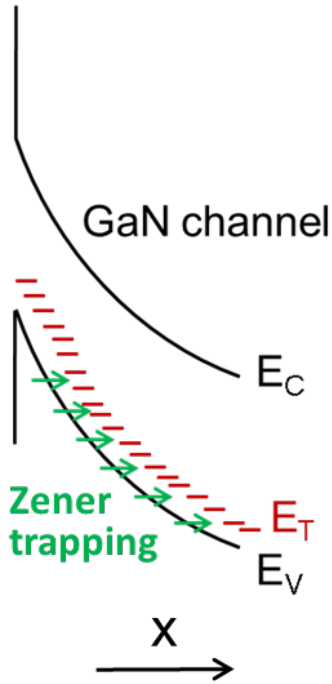
ΔV_T mechanism



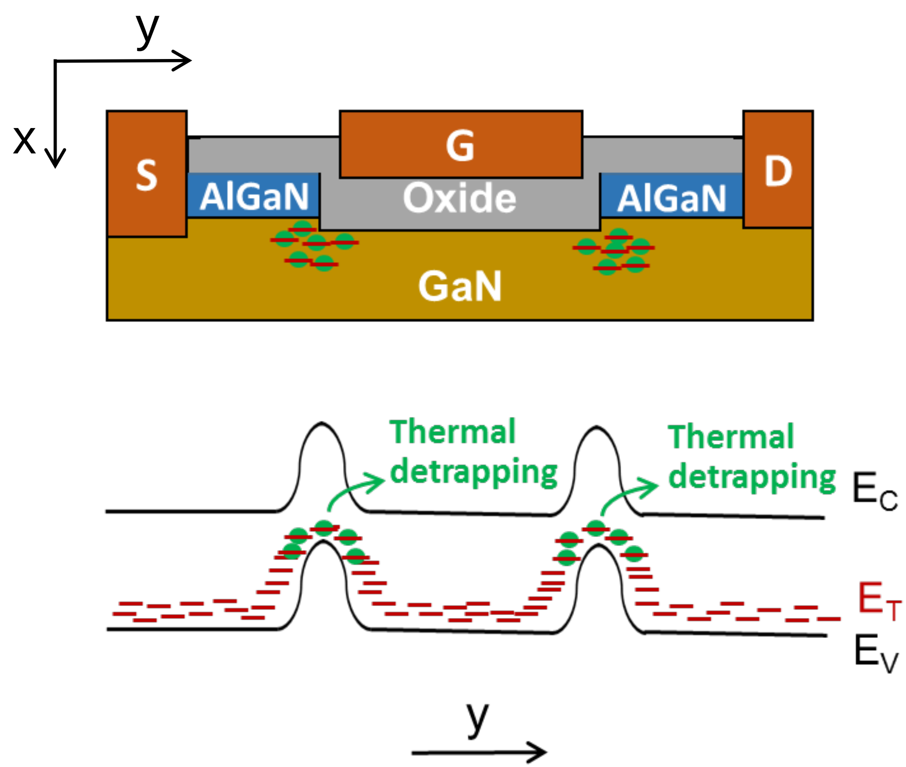
[Jin, IEDM 2013]

Regime 2 (mid-stress)

ΔV_T mechanism



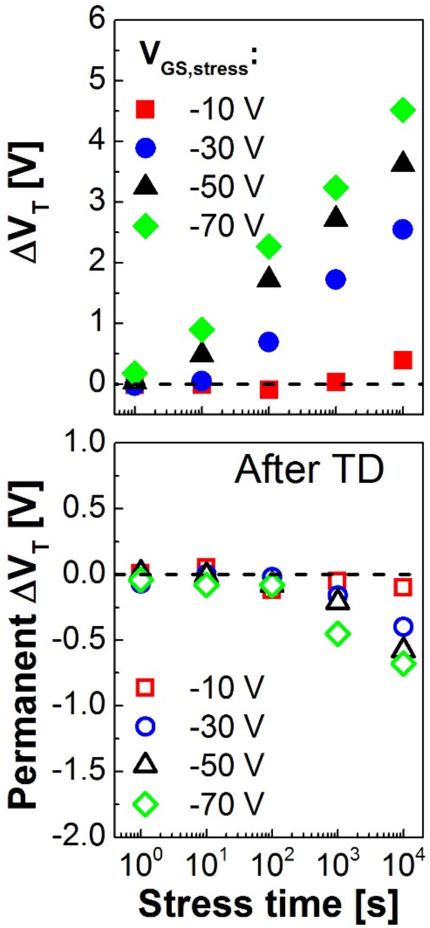
[Jin, IEDM 2013]



- **High field at edges of gate → Zener trapping in GaN substrate**
- **Energy bands at surface of GaN channel ↑ → Positive ΔV_T, ΔS**
- **Thermal process effective in electron detrapping**

Regime 3 (high-stress)

t_{stress} evolution of ΔV_T at RT

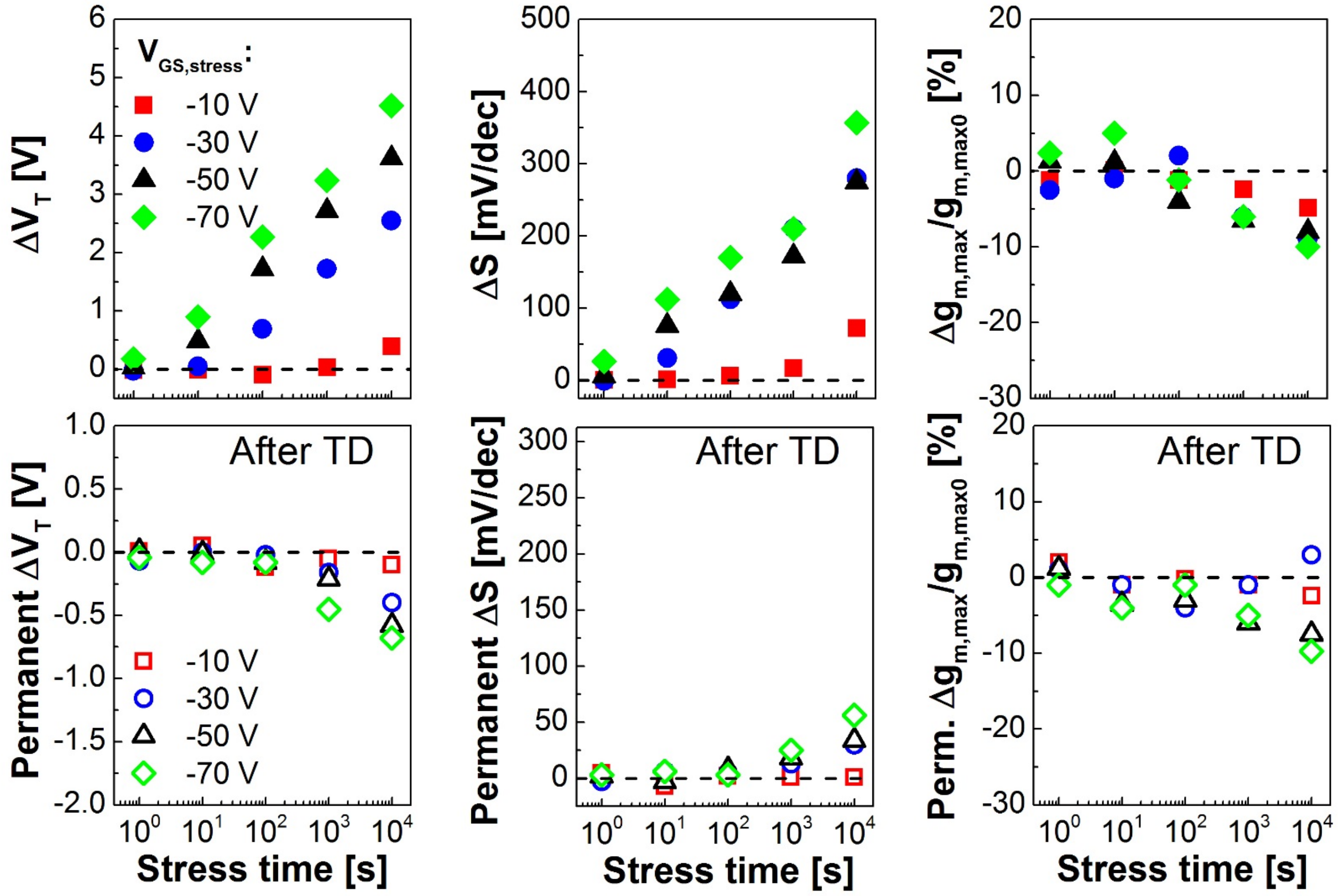


→ **Similar to regime 2**

→ **Additional permanent negative ΔV_T**

Regime 3 (high-stress)

t_{stress} evolution of ΔV_T at RT

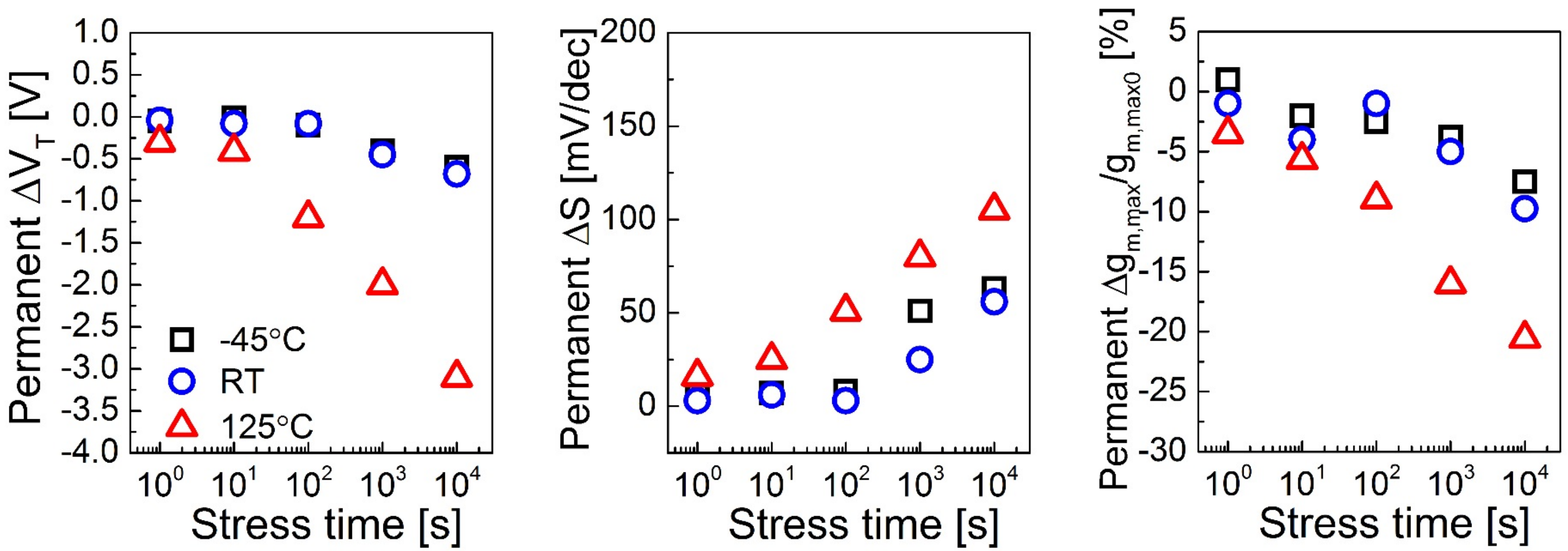


- t_{stress} ↑, $|V_{GS,stress}|$ ↑ → permanent $|\Delta V_T|$↑, ΔS ↑ and $|\Delta g_{m,max}|$↑

Regime 3 (high-stress)

Temperature dependence

$V_{GS,stress}$ = -70 V, t_{stress} = 1 – 10,000 s

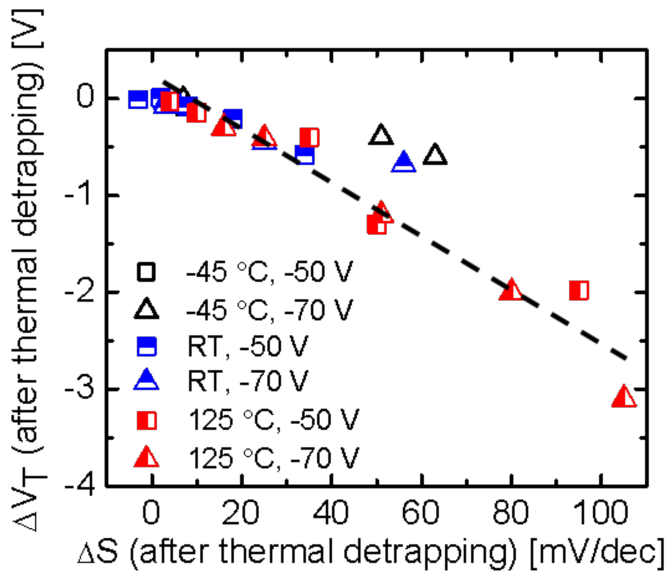


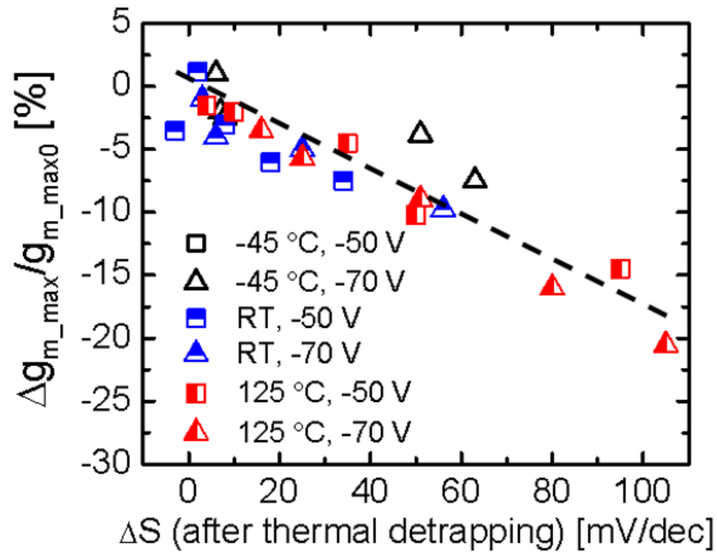
- **T ↑ → permanent $|\Delta V_T|$ ↑, ΔS ↑ and $|\Delta g_{m,max}|$ ↑**

Regime 3 (high-stress)

Correlation of permanent ΔV_T , ΔS and $\Delta g_{m,max}$

Measurements at RT



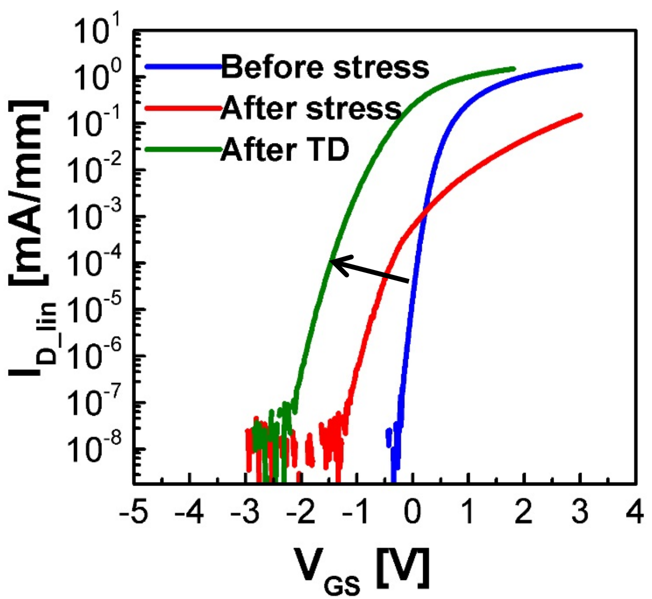


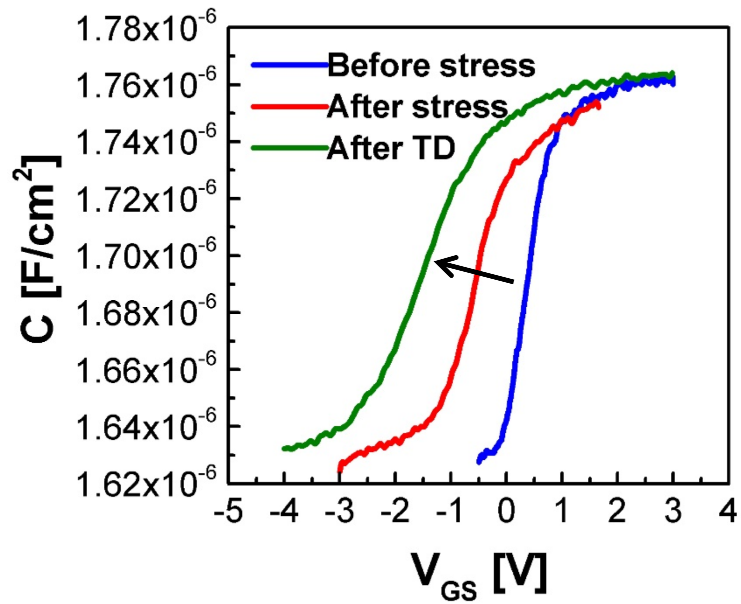
- **Permanent ΔV_T , ΔS and $\Delta g_{m,max}$ well correlated**

Regime 3 (high-stress)

I_D-V_{GS} and C_G-V_G characteristics

$V_{GS,stress}$ = -70 V, t_{stress} = 500 s, T = 125°C



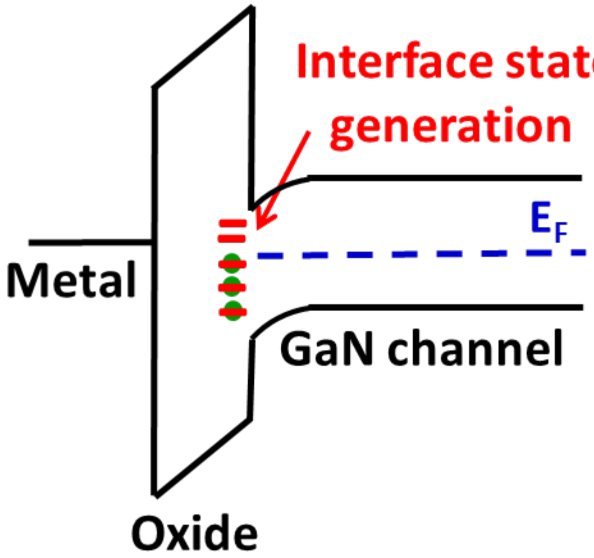


- Prominent ΔV_T , ΔS and $\Delta g_{m,max}$ correlate with a softening of C-V characteristics around threshold

Regime 3 (high-stress)

ΔV_T Mechanism

- **Interface state generation under high gate stress**



- **Well-studied mechanism in Si MOS system [Schroder, JAP 2007]**

Outline

1. Motivation
2. Experimental setup
3. Three regimes of NBTI
4. **Summary of contributions**

NBTI of GaN MOSFETs

Identified three degradation mechanisms:

- **Regime 1 (low-stress)**
  - **Observation: small, recoverable negative ΔV_T**
  - **Mechanism: electron detrapping from pre-existing oxide traps**

- **Regime 2 (mid-stress):**
  - **Observation: recoverable positive ΔV_T and ΔS**
  - **Mechanism: Zener trapping in channel under edges of gate**

- **Regime 3 (high-stress):**
  - **Observation: negative, non-recoverable ΔV_T , ΔS and $\Delta g_{m,max}$**
  - **Mechanism: interface state generation**